

PATENT ABSTRACTS OF JAPAN

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(71)Applicant : NEC CORP

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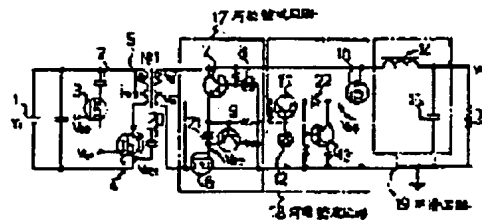
(72)Inventor : NEGOME TAKETO

(54) SWITCHING POWER SUPPLY

(57)Abstract:

PROBLEM TO BE SOLVED: To enable the enhancement of the power conversion efficiency of a switching power supply, by using FET for synchronous rectification and a circuit for making gate drive waveform constant, and further adding a high-speed off-circuit when the gate waveform is off.

SOLUTION: In a low-loss gate drive circuit using a synchronous rectification circuit, FET's 6, 10 are fed with a gate voltage obtained by stabilizing the secondary winding voltage of a transformer 5 through the transistors 7, 10 for clamp and the diodes 8, 12 in a waveform shaping circuit. A diode for circuit interruption is connected with the gate of the FET 10 for reflux in a synchronous rectification circuit 18 between a transistor 11 for clamp and a transistor 13 for discharge in order to discharge the charges in the gate capacitance through the transistor 13 at high speed. As a result, when the gate voltage is off, the voltage is quickly discharged through transistors 9, 13, and the diodes built in the FET's are turned off before they are turned on. Thereby loss is reduced. As a result, the risk of gate breakdown can be reduced.



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[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] Especially this invention relates to the efficient-ized switching power supply which used synchronous detection about switching power supply.

[0002]

[Description of the Prior Art] Conventionally, this kind of gate drive circuit for synchronous detection of low loss is used in switching power supply for the purpose of reduction of power consumption, or improvement in the reliability of a device.

[0003] For example, to JP.8-336282.A, a synchronous detection gating waveform is operated orthopedically, the danger of gate destruction is abolished to it, and the technology of also reducing loss of a gate drive circuit is indicated.

[0004]

[Problem(s) to be Solved by the Invention] However, the conventional example on ** had the **** fault shown below.

[0005] The 1st trouble has the trouble that the time of "off" of a gate drive voltage waveform is lost late, in a Prior art.

[0006] The reason is because the built-in diode of FET for synchronous detection "turns on" on.

[0007] this invention is made in order to cancel the above-mentioned fault which is inherent in a Prior art in view of the conventional above-mentioned actual condition, therefore the purpose of this invention reduces loss of FET for synchronous detection, and the new switching power supply which made it possible to raise the power conversion efficiency of switching power supply is offered -- it is in things

[0008] Other purposes of this invention are to abolish the danger of gate destruction of FET for synchronous detection.

[0009]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, using a circuit where FET for synchronous detection and a gate drive wave become fixed, further, the switching power supply concerning this invention adds the circuit which carries out "" at high speed at the time of gating waveform "off", and is constituted at it.

[0010] In this invention, if the gate drive wave of FET for synchronous detection is fixed and it fixes also in the input minimum voltage - input maximum voltage, loss of FET can be reduced.

[0011] Moreover, the danger of gate destruction also disappears.

[0012] By carrying out "off" [of the synchronous detection FET gate drive wave] at high speed, before diode with built-in FET "turns on" on, "" can be carried out, and it becomes possible to reduce loss.

[0013]

[Embodiments of the Invention] Next, this invention is explained in detail, referring to a drawing about the gestalt of the 1 desirable operation.

[0014] Drawing 1 is the circuitry view showing the gestalt of 1 operation of this invention.

[0015] With reference to drawing 1, the gestalt of the 1 operation by this invention consists of the DC input voltage 1, the main switching elements (MOS FET) 3 and 4, a transformer 5, synchronous detection circuits 17 and 18, a smoothing circuit 19, and load 16 grade.

[0016] Drawing 2 is a timing diagram which shows operation of the gestalt of the 1 operation by this invention shown in drawing 1.

[0017] The main switching elements (MOS FET) 3 and 4 are driven by the gate voltage V_g of MOS

[0018] Period t₁ - t₂ the primary side main switching element 4 turns on, the gate voltage V_g of FET6 "turned on" on, let the smoothing circuit 19 pass by the gate voltage of FET6 for secondary synchronous detection, and was rectified to the load 16 It is impressed.

[0019] Period t₂ - t₃ Exciting current im to which the main switching elements 3 and 4 are "off"

periods, and are flowing to the transformer 5 in the meantime. The charge and discharge of the parasitic capacitance 20 are carried out by peak value I_{p+} .

[0020] Period $t_3 \sim t_4$ The main switching element 4 is the period when the main switching element 3 is "turned on" in "OFF", and the ends of secondary **** of a transformer 5 are clamped by the clamping circuit which consists of the main switching element 3 and a capacitor 2 in the meantime.

[0021] By the gate voltage of FET10 for a rotary flow of a secondary, FET10 "turns on" on, the load current returns through FET10, and this period is the rectification voltage V_o to a load 16. It is impressed.

[0022] Next, the gate drive circuit of low loss using a synchronous detection circuit is explained with reference to drawing 1.

[0023] Here, the place which should be observed is the point that the stable gate voltage is applied by the waveform shaping circuit secondary **** voltage of a transformer 5 was constituted by the transistor 7 and diode 8 (a transistor 11, diode 12) rather than was impressed to FET6 and FET10 as it was.

[0024] That is, the waveform shaping circuit which changes from the transistor 7 for a clamp which clamps the gate voltage of FET6 to the zener diode 8 which generates a constant voltage, and below the fixed voltage that this zener diode 8 outputs is prepared in the gate circuit of FET6 for synchronous detection of the synchronous detection circuit 17.

[0025] On the other hand, the transistor 11 for a clamp which clamps the gate voltage of FET10 is connected to the zener diode 12 which generates a constant voltage, and below the fixed voltage that this zener diode 12 outputs at the gate circuit of FET10 for a rotary flow of the synchronous detection circuit 18.

[0026] Usually, when it is the conventional example in which a direct gate voltage is immediately applied to FET from the **** voltage of a transformer 5 (drawing 3), it is V_{DS1} of the primary side main switching element 4 in change of input voltage. Voltage changes. That is, if it is low if input voltage is low, and input voltage is high, high voltage will occur and the **** ratio of a transformer 5 will be impressed by the secondary. If this **** voltage is high, the gate voltage of FET 6 and 10 for synchronous detection will also become high, loss of FET 6 and 10 will increase, and efficiency will fall. Moreover, if a gate voltage becomes high, the problem of the danger of FET6 and gate destruction of ten will also be produced.

[0027] Another feature had the late time of "off" of a gate voltage in the conventional FET gate drive circuit for synchronous detection (technology indicated by JP,8-336282,A), and it was one of the causes of loss (refer to [drawing 4 VG1' and] VG4').

[0028] In order to solve this, this invention is a circuit aiming at drawing out voltage quickly at the time of "off" of a gate voltage, carrying out "" at high speed, before the diode built in FET "turns on" on, and reducing loss with the transistor 9 of drawing 1 (13).

[0029] That is, the diode 21 for circuit cutting is connected between the connection of the transistor 9 for electric discharge which draws out the charge charged by the gate capacitance of FET6 at high speed in the gate of FET6 for a synchronization of the synchronous detection circuit 17 (it is made to discharge), and the base of this transistor 9 and the gate of FET6, and the connection of the emitter of the transistor 7 for a clamp of a waveform shaping circuit, and the base of the transistor 9 for electric discharge.

[0030] Similarly, the diode 22 for circuit cutting is connected to the gate of FET10 for a rotary flow of the synchronous detection circuit 18 between the connection of the transistor 13 for electric discharge which draws out the charge charged by the gate capacitance of FET10 at high speed (it is made to discharge), and the base of this transistor 13 for electric discharge and the gate of FET10 and the connection of the emitter of the transistor 11 for a clamp of a waveform

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[0032] It is the output voltage V_s of a transformer 5 now for referring to drawing 1 and drawing 2. - Time t_1 If set to 0V, the emitter of a transistor 11 will be set to 0V through the collector of the transistor 11 "turned on", and the base of the transistor 13 for electric discharge connected

with this emitter will also be set to 0V. Consequently, a transistor 13 will be in an "ON" state, the gate of FET10 is grounded, and the charge charged by the gate capacitance of FET10 is drawn out at high speed (it discharges). When a transistor 13 "turns on" on, diode 22 works so that the emitter of a transistor 11 and the gate of FET may be cut on a circuit, and promotes "ON" operation of a transistor 13. "ON" operation of the diode built in FET10 is prevented as a result of the above-mentioned operation.

[0033] Since it operates like [the transistor 9 for electric discharge, and the diode 21 for circuit cutting] the above, the explanation is omitted.

[0034] Moreover, in this invention, the switching circuit by the side of primary may use not only the switching circuit of an active clamp form as shown in drawing 1 but half bridge type, and stone forward type or Class E resonance type.

[0035]

[Effect of the Invention] this invention is constituted like the above and acts, and according to this invention, an effect as taken below is acquired.

[0036] The 1st effect can gather efficiency by using a transistor and zener diode for a synchronous detection gate drive circuit. Moreover, the danger of gate destruction can also be abolished.

[0037] Since a gate voltage is regularity (pressed down low) even if input voltage is high, the reason is because loss can be reduced and there is also no elevation of a gate voltage.

[0038] The 2nd effect can gather efficiency by using the transistor for electric discharge for a synchronous detection gate drive circuit.

[0039] The reason is because "off" [of the gate voltage] can be carried out at high speed, diode with built-in FET "does not turn [but] on" on and loss can be reduced.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the detailed circuitry view showing the gestalt of 1 operation of this invention.

[Drawing 2] It is the timing chart which shows the wave of each part of composition of having been shown in drawing 1 .

[Drawing 3] It is the conventional circuit diagram.

[Drawing 4] It is drawing showing the wave of each part of the circuit shown in drawing 3 .

[Description of Notations]

1 -- Input power

2 15 -- Capacitor

3, 4, 6, 10 -- MOS FET

5 -- Transformer

7, 9, 11, 13 -- Transistor

8 12 -- Zener diode

14 -- Choke coil

16 -- Load

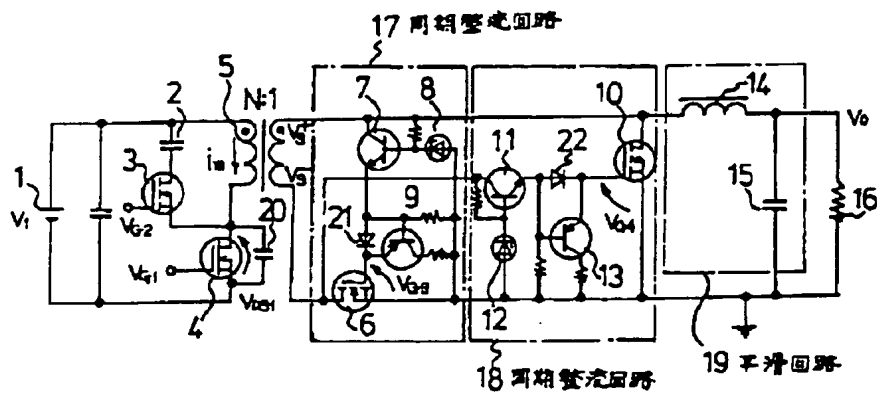
17 18 -- Synchronous detection circuit

19 -- Smoothing circuit

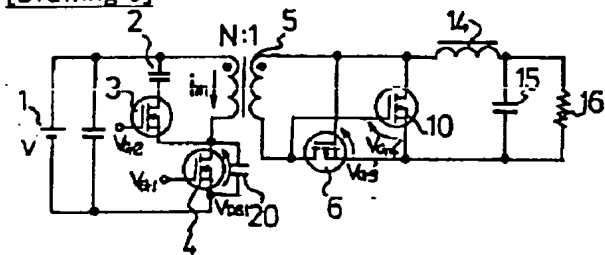
20 -- Parasitic capacitance

21 22 -- Diode

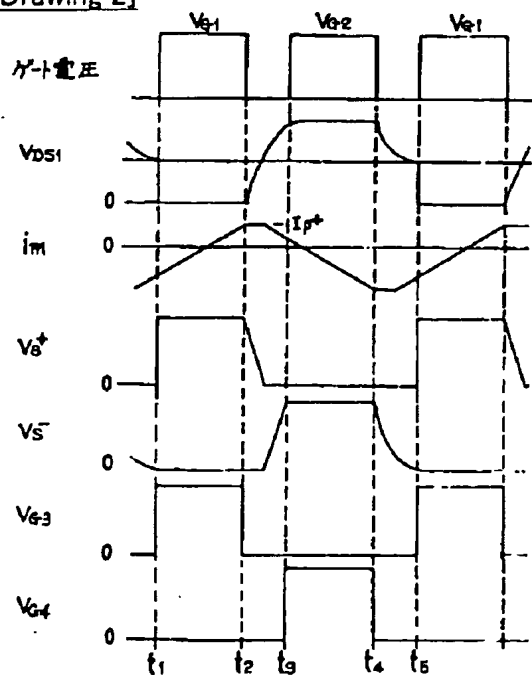
[Drawing 1]

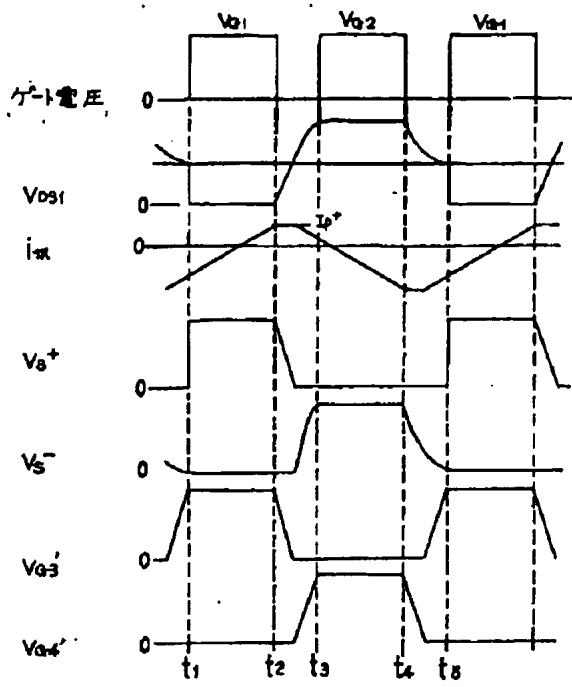


[Drawing 3]



[Drawing 2]





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(71)出願人 000004237

日本電気株式会社

東京都港区芝五丁目7番1号

(72) 发明者 根米 健人

東京都港区芝五丁目7番1号日本電気株式
会社内

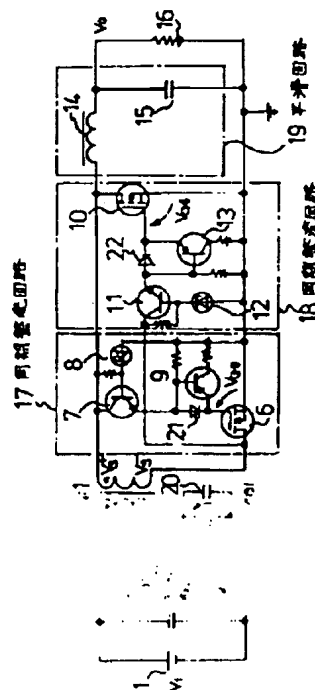
(74) 代理人 弁護士 熊谷 雄太郎

(54) 【発明の名称】 スイッチング電源

(57) 【要約】

【課題】 同期整流用FETの内蔵ダイオードがゲート電圧のデッドタイム時に“オン”してしまうために、FETのゲートドライブ電圧波形の“オフ”時間が遅くなり、それが損失になっていた

【解決手段】 同期整流用MOS-FET6のゲートに、FET6のゲート容量にチャージされた電荷を高速に引き抜く放電用トランジスタ9と同路切断用ダイオード1を接続する。同様に環流用MOS-FET10のゲートに、同様の機能を有するトランジスタ13とダイオード22を接続する。



【特許請求の範囲】

【請求項1】 直流入力電圧をトランスの1次巻線に供給し、周期的に“オン”、“オフ”するスイッチング電源において、このスイッチング手段が“オフ”する間にトランスの1次巻線の両端の電圧を制限するクラブ手段と、前記トランスの2次巻線出力を整流・平滑する整流・平滑手段とを有し、

前記整流・平滑手段に、同期整流方式の整流・平滑回路を用い、前記同期整流・平滑回路の同期整流用電界効果トランジスタのゲートと前記トランスの2次巻線の一端との間に第1の波形整形手段が設けられていることを特徴とするスイッチング電源、

【請求項2】 前記同期整流・平滑回路の環流用電界効果トランジスタのゲートと前記トランスの2次巻線の他端との間に第2の波形整形手段が設けられていることを更に特徴とする請求項1に記載のスイッチング電源、

【請求項3】 前記第1及び第2の波形整形手段は、クランプ用トランジスタと、定電圧を発生するツェナダイオードとを有することを更に特徴とする請求項2に記載のスイッチング電源、

【請求項4】 前記同期整流用電界効果トランジスタのゲートに、前記同期整流用電界効果トランジスタのゲート容量にチャージされた電荷を高速に放電させる第1の放電手段を設けたことを更に特徴とする請求項1に記載のスイッチング電源、

【請求項5】 前記環流用電界効果トランジスタのゲートに、該環流用電界効果トランジスタのゲート容量にチャージされた電荷を高速に放電させる第2の放電手段を設けたことを更に特徴とする請求項4に記載のスイッチング電源、

【請求項6】 前記第1の放電手段は、前記同期整流用電界効果トランジスタのゲートに接続された第1の放電用トランジスタと、第1の回路切断用ダイオードとを有することを更に特徴とする請求項4に記載のスイッチング電源、

【請求項7】 前記第2の放電手段は、前記環流用電界効果トランジスタのゲートに接続された第2の放電用トランジスタと、第2の回路切断用ダイオードとを有することを更に特徴とする請求項5に記載のスイッチング電源、

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、スイッチング電源に関し、特に、同期整流を用いた高効率化スイッチング電源に関する。

【0003】例えば、特開平8-336282号公報には、同期整流ゲート波形を整形し、ゲート破壊の危険性を無くし、ゲートドライブ回路の損失も低減する技術が記載されている。

【0004】

【発明が解決しようとする課題】しかしながら、従来例には下記に示す如き欠点があった。

【0005】第1の問題点は、従来の技術においては、ゲートドライブ電圧波形の“オフ”時が遅く損失になるという問題点がある。

【0006】その理由は、同期整流用FETの内蔵ダイオードが“オン”してしまうためである。

【0007】本発明は従来の上記実情に鑑み、従来の技術に内在する上記欠点を解消する為になされたものであり、従って本発明の目的は、同期整流用FETの損失を低減し、スイッチング電源の電力変換効率を向上させることを可能とした新規なスイッチング電源を提供することにある。

【0008】本発明の他の目的は、同期整流用FETのゲート破壊の危険性をなくすることにある。

【0009】

【課題を解決するための手段】上記目的を達成する為には、本発明に係るスイッチング電源は、同期整流用FET、ゲートドライブ波形が一定となるような回路を用い、さらにゲート波形“オフ”時に高速に“オフ”する回路を付加して構成される。

【0010】本発明において、同期整流用FETのゲートドライブ波形を一定にし、入力最低電圧～入力最大電圧においても一定にすれば、FETの損失を低減することができる。

【0011】また、ゲート破壊の危険性もなくなる。

【0012】同期整流FETゲートドライブ波形を高速に“オフ”することにより、FET内蔵ダイオードが“オン”する前に“オフ”することができ、損失を低減することが可能となる。

【0013】

【発明の実施の形態】次に本発明を一例好ましい一実施の形態について図面を参照しながら詳細に説明する。

【0014】図1は本発明の一実施の形態を示す回路構成図である。

【0015】図1を参照するに、本発明による一実施の形態は、DC入力電圧1、メインスイッチング素子MOS-FET3、4、トランス5、同期整流回路17、18、平滑回路19、負荷16等にて構成されている。

電力の低減や機器の信頼性の向上を目的として用いられている。

に、ゲートドライブ電圧を一定に保ち、ゲート破壊の危険性をなくし、ゲートドライブ回路の損失も低減する技術が記載されている。

ものであり、本発明によれば以下に示すような効果が得られる。

【0036】第1の効果は、同期整流ゲートドライブ回路にトランジスタとツェナダイオードを用いることにより、効率を上げることができる。また、ゲート破壊の危険性もなくすることができる。

【0037】その理由は、入力電圧が高くても、ゲート電圧が一定（低）おさえられる）であるために、損失が低減でき、ゲート電圧の上昇もないためである。

【0038】第2の効果は、同期整流ゲートドライブ回路に放電用トランジスタを用いることにより効率を上げることができる。

【0039】その理由は、ゲート電圧を高速に“オフ”することができ、FET内蔵ダイオードが“オン”せず、損失を低減できるためである。

【図面の簡単な説明】

【図1】本発明の一実施の形態を示す詳細回路構成図である。

【図2】図1に示された構成の各部の波形を示すタイミングチャートである。

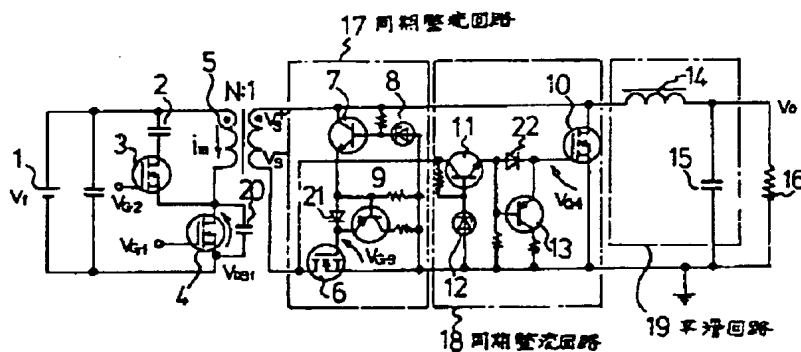
【図3】従来の回路図である。

【図4】図3に示した回路の各部の波形を示すタイミングチャートである。

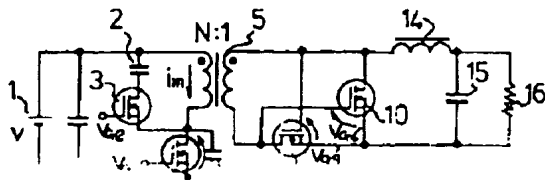
【符号の説明】

- 1…入力電源
- 2…1μ…コンデンサ
- 3、4、6、10…MOS-FET
- 5…トランス
- 7、9、11、13…トランジスタ
- 8、12…ツェナダイオード
- 14…チョークコイル
- 16…負荷
- 17、18…同期整流回路
- 19…平滑回路
- 20…寄生容量
- 21、22…ダイオード

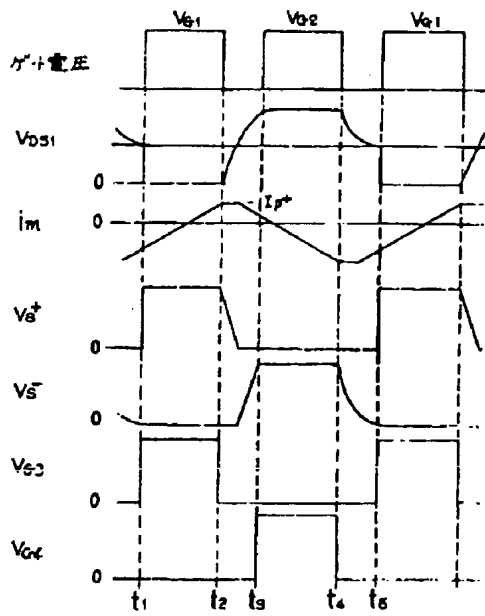
【図1】



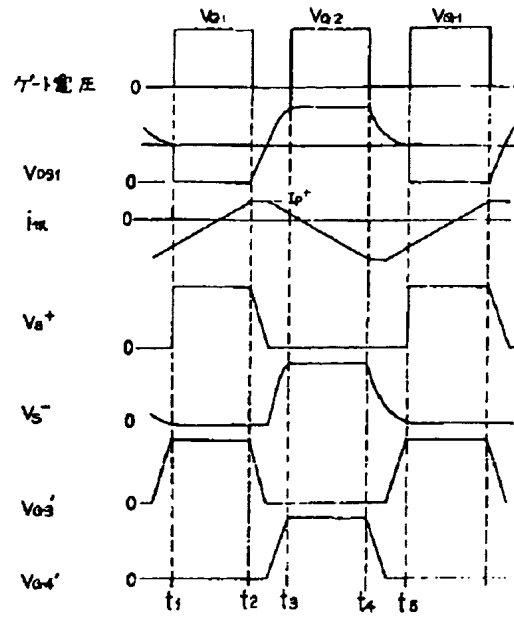
【図3】



【図2】



【図3】



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